REMARKS

Claims 1-20 are now present in this application.

The Abstract and claims 1, 6, 7, 10, 11, 15, 16, and 19 have been amended, claims 4, 5, and 14 have been cancelled without prejudice or disclaimer of the subject matter contained therein, and claim 20 has been presented. Reconsideration of the application, as amended, is respectfully requested.

The abstract stands objected to for certain informalities. In view of the foregoing amendments, it is respectfully submitted that these informalities have been addressed. Accordingly, reconsideration and withdrawal of any objection to the abstract are respectfully requested.

The drawings stand objected to for certain informalities. It is respectfully submitted that replacement drawing sheets for Figs. 2 and 3 are being submitted concurrently herewith, in which the previously omitted nodes have been added and the gates of two PMOS and one NMOS in the driving circuit have been amended to be connected with each other. Reconsideration and withdrawal of any objection to the drawings are respectfully requested.

Claims 1-13 stand rejected under 35 USC 103 as being unpatentable over the Applicant's admitted prior art in view of KER et al., U.S. Patent 5,959,820. This rejection is respectfully traversed.

Claim 1 of the present application recites an electrostatic discharge protection device located between a pad and an internal circuit, and coupled between a first power wire and a second power wire, comprising a switching circuit for outputting an enable signal when receiving a detecting result signal; a driving circuit coupled to the switching circuit for outputting a ground level signal when receiving the enable signal; a voltage detecting device including at least one serial diode connected between the first power wire and the switching circuit, and outputting the detecting result signal when a voltage level of the first power wire reaches a first predetermined voltage level; a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level; a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level; and a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third

controlling gate connected to the driving circuit and is turned on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the ground level signal.

Claim 11 of the present application recites an electrostatic discharge protection device located between a pad and an internal circuit, and is coupled to a first power wire, a second power wire, and a third power wire, comprising: a switching circuit for outputting an enable signal when receiving a detecting result signal; a driving circuit coupled to the switching circuit and the third power wire for outputting a ground level signal when receiving the enable signal; a voltage detecting device including at least one serial diode connected between the third power wire and the switching circuit, and outputting the detecting result signal when a voltage level of the third power wire reaches a first predetermined voltage level; a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level; a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage

level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level; and a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate connected to the driving circuit and is turned on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the ground level signal.

The Applicant's admitted prior art discloses an electrostatic discharge protection device located between a pad and an internal circuit, and is coupled to a first power wire, a second power wire, and a third power wire, comprising: a switching circuit for outputting an enable signal when receiving a detecting result signal; a driving circuit coupled to the switching circuit and the third power wire for outputting a ground level signal when receiving the enable signal; a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level; a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third predetermined voltage level lower

than the second predetermined voltage level; and a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate connected to the driving circuit and is turned on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the ground level signal.

KER et al. teaches a voltage based ESD detection circuit and provides multiple ways for implantation of such ESD detection circuits including a diode string. The ESD detection circuit in KER et al. detects the electrostatic discharge happening at the power supplies and triggers the control gates of the cascade LVSCR for dissipating the electrostatic discharge.

The ESD detection circuit in KER et al. accelerates the turn on of the cascade LVSCR. In KER et al., the ESD event ~~is~~ happened at the power wire, and the voltage based ESD detection circuit detects the voltage level of the power wire, and turns on the control gates of the cascade LVSCR for dissipating the electrostatic discharge.

However, KER et al. does not disclose a voltage detecting device including at least one serial diode connected between the power wire and the switching circuit, outputting the detecting result signal when a voltage level of the first power wire reaches a first predetermined voltage level and a second switch coupled to

the connection point between the pad and the internal circuit is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level. Here, the second predetermined voltage level is the voltage level of electrostatic discharge. Therefore, the voltage detecting device outputs the detecting result signal when the voltage level of the first power wire reaches a first predetermined voltage level by the leakage current through the second switch (PMOS transistor) when the voltage level of the pad reaches the second predetermined (ESD) voltage level.

Neither the Applicant's admitted prior art nor KER et al. teaches or suggests a voltage detecting device including at least one serial diode connected between the power wire and the switching circuit, outputting the detecting result signal when a voltage level of the first power wire reaches a first predetermined voltage level and a second switch coupled to the connection point between the pad and the internal circuit is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level. In KER et al., the ESD happens on the power wire of the circuit. Contrarily, the ESD happens on the pad of the circuit disclosed by the Applicant's admitted prior art. Thus, persons having ordinary skill in the art cannot add the voltage based ESD detection circuit in KER et al.

between the power wire and the switching circuit of the Applicant's admitted prior art.

The problem of the Applicant's admitted prior art is that the third switch (the PMOS transistor M52 or M53 shown in FIG. 3) might be turned on before the first switch (the NMOS transistor M50 or M51 shown in FIG. 3) breaks down. Therefore, massive ESD current flows to ground through the third switch and prevents the first switch from breaking down, decreasing ESD current discharge ability.

Thus, the present invention provides a voltage detecting device including at least one serial diode connected between the power wire and the switching circuit, outputting the detecting result signal when a voltage level of the first power wire reaches a first predetermined voltage lower than the second predetermined voltage (ESD voltage).

Thus, the purpose of the present invention and KER et al. are completely different. In KER et al., as the voltage detecting device only detects the ESD event happened on the power wire, and does not detect the ESD event which happened on the pad by sensing the voltage level of the power wire, persons having ordinary skill in the art cannot infer the present invention by combining the Applicant's admitted prior art with KER et al.

In view of the foregoing amendments and remarks, it is respectfully submitted that the electrostatic discharge protection device disclosed in independent claims 1 and 11 of the present application, as well as their dependent claims, is neither taught nor suggested by the prior art utilized by the Examiner. Accordingly, reconsideration and withdrawal of the 35 USC 103 rejection are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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